IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning on page 2, line 29 is deleted as follows:

~~Thicker adsorbed layers etch the underlying layer more quickly as a cost of having more surface tension. Therefore, a typical approach to reduce surface tension is to maintain a very thin layer of adsorbed material on the surface of the layer being etched. Accordingly, such an approach requires more vapor etching tools to decrease the time to perform vapor etch operations. In other words, more vapor etching tools are added to operate in parallel. This can be prohibitive in terms of cost and the footprint (space) needed to accommodate such tools.~~

The paragraph beginning on page 10, line 7 is amended as follows:

In an embodiment, the etch initiator source 110 inputs an etch initiator composition into the mix unit 112. A surface tension lowering agent source 106 is coupled to input a surface tension lowering agent into mix the unit 112. The surface tension lowering agent is introduced into the vapor to lower the surface tension on the surface of the layer being etched. The thickness of the adsorbed layer of etchant on the surface of the layer being etched may therefore be thicker in comparison to the thickness maintained during conventional etching processes.

The paragraph beginning on page 10, line 27 as follows:

The mix unit 112 is coupled to a valve 114. The valve 114 is coupled to the inlet 107. Accordingly, the valve 114 (when opened) releases the mixed vapor into the vapor etch chamber 102. As described in more detail below, the mixed vapor etches at least one layer of the semiconductor substrate 102. Moreover, the surface tension lowering agent combines with the product of the vapor etch operation to generate an ~~absorbed~~ adsorbed layer on the surface of the layer being etched.

The paragraphs beginning on page 12, line 20 as follows:

Figure 3 illustrates a fabrication of the semiconductor substrate of Figure 2 at a first stage, according to one embodiment of the invention. As shown, the semiconductor substrate

102 is surrounded by a mixed vapor 310. A vapor phase etch operation is performed to remove the insulator material 218 using the mixed vapor 310. The mixed vapor may be comprised of a number of different substances in combination with a surface tension lowering agent (as described above in conjunction with Figure 1 above). As shown, an ~~absorbed~~ adsorbed layer 302 is formed on the top of the insulator material 218. The ~~absorbed~~ adsorbed layer 302 includes the surface tension lowering agent in combination of the results of the vapor phase etch.

Figure 4 illustrates a fabrication of the semiconductor substrate of Figure 2 at a second stage, according to one embodiment of the invention. As shown, the semiconductor substrate 102 is surrounded by the mixed vapor 310. The vapor phase etch operation continues to remove the insulator material 210 using the mixed vapor 310. The ~~absorbed~~ adsorbed layer 302 remains on the top of the insulator material 218.

The paragraph beginning on page 17, line 16 as follows:

Thus, methods, apparatuses and systems for different embodiments for semiconductor fabrication that includes surface tension control have been described. As illustrated, embodiments of the invention allow for a faster etch rate in comparison to conventional vapor phase etch operations. For example, in one embodiment, a vapor phase etch operation is performed on a material adjacent to a memory container having a side wall that includes a double-sided capacitor. As described above, such a container includes fine structures which are relatively close together that need to remain isolated from each other. Accordingly, alterations/damages (such as bending) of this side wall needs to be reduced in order to preclude the structures therein from bending and/or coming into contact with each other. As described above, embodiments of the invention introduce a surface tension lowering agent into the vapor, thereby lowering the surface tension that is resident on the surface of the layer being etched because of the ~~absorbed~~ adsorbed layer. Therefore, the ~~absorbed~~ adsorbed layer on the surface of the layer being etched may be thicker (in comparison to typical approaches) while lowering the amount of surface tension that maybe present.